REMARKS

Claims 1-35 remain pending in the application. No amendments to the claims are presented at this time.

Claims 1-5, 8-13, 15-20 and 22-35 were rejected under 35 U.S.C 102(e) as being anticipated by Ooishi. Applicants respectfully traverse.

Independent claims 1, 10, 25 and 32 each include a limitation relating to the formation of a differential amplifier circuit for read data output generation wherein the differential amplifier includes components of the addressed memory cell itself. For example, in claim 1, the differential amplifier is claimed to be comprised of the reference cell (comprising a select transistor and resistive element), the transistor (coupled between the bit line and first reference voltage) and the addressed memory cell (comprising a select transistor and resistive element). In claim 10, the differential amplifier is claimed to be comprised of load components, the reference cell (comprising a select transistor and resistive element), the transistor (coupled between the bit line and first reference voltage) and the addressed memory cell (comprising a select transistor and resistive element). In claim 25, the differential amplifier is claimed to be comprised of the reference cell, the transistor (coupled between the bit line and first reference voltage) and the addressed memory cell. Lastly, in claim 32, the differential amplifier is claimed to be comprised of the reference cell, the transistor (coupled between the data line and reference voltage) and the selected memory cell.

The Ooishi reference teaches the use of a sense amplifier circuit (components 110, 120, 130 and 150) for generating the data out from the read memory cell. It is clear in Ooishi that the sense amplifier circuit is discrete from the memory array (see, dotted outline 100). In other

words, there is no indication in Ooishi that the sense amplifier circuit, in general, or the initial amplifiers 110/120, in particular, are in any way formed from components of the addressed memory cell itself, as is specifically claimed by Applicant. In view of the foregoing, Applicant respectfully submits that the Ooishi teachings are irrelevant to the claimed invention, and further that Ooishi teaches away from the claimed invention by describing a discrete sense amplifier circuit for data out reads.

An advantage of the Applicant's circuit over circuits like that taught by Ooishi, is that Applicant's data output circuit does not require the use of a sense amplifier (see, allowed claims 7 and 21). The differential amplifier formed in part from components of the addressed memory cell itself serves the read function and obviates any need for a separate sense amplifier to read the bit lines and drive the data output.

Applicant respectfully submits that the application is in condition for favorable action and allowance.

Respectfully submitted,
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